Modeling for Intra–Chip Optical Interconnects

Problem

•CMOS thermal environment:
hot (> 125 C and variable (± 10 C)

Objective

•Couple thermal CMOS models with circuit-level VCSEL models

• Integrate models with standard system design tools for higher functionality VSCEL-based circuits

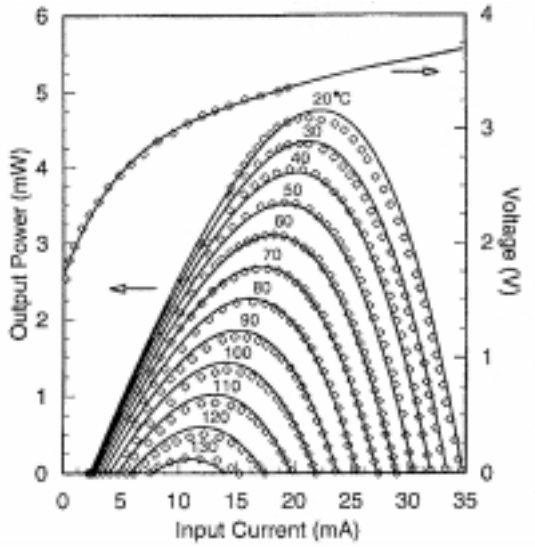
Approach

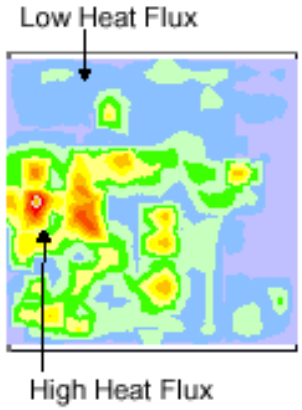
•Combine multiple time and frequency domain measurements with a fast non-linear fitting routine

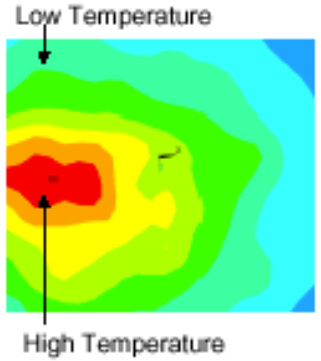
•Use simple polynomial for temperature dependence

• Partners: Motorola, Sun

Measured and modeled I-V and L-I curves as a function of temperature







Thermal flux and temperature of an Intel processor (from Intel).

G. Papen

Coding for Intra–Chip Optical Interconnect

Problem

•Designing lasers that can operate "open-loop" with CMOS is hard

Objective

•Use coding to overcome physical limitations of devices (variable thresholds, slopes efficiencies, jitter, etc.)

Approach

•Leverage coding work on multimode fiber

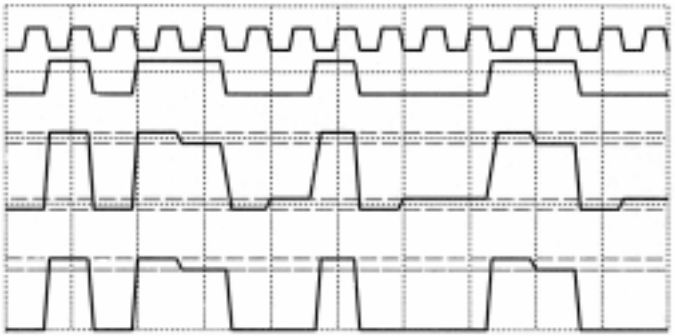
•Trade bandwidth for redundancy

•Use simplified forms of forward error correction (FEC) codes developed for 1000 base-T.

• Partners: Agilent, Sun

G. Papen

3.3 V VCSEL CMOS driver output



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